ABSTRACT OF THE DISCLOSURE

In an output buffer apparatus including a main-buffer circuit including a plurality of first transistors each connected between a first power supply terminal and an output terminal and a plurality of second transistors each connected between a second power supply terminal and the output terminal, and a pre-buffer circuit including a plurality of first pre-drivers each driving one of the first transistors in accordance with a data signal and a plurality of second pre-drivers each driving one of the second transistors in accordance with the data signal, a plurality of first sequential circuits are provided for receiving first impedance adjusting signals in synchronization with the data signal to turn ON the first pre-drivers, and a plurality of second sequential circuits are provided for receiving second impedance adjusting signals in synchronization with the data signal to turn ON the second pre-drivers.